REMARKS

This is a full and timely response to the outstanding final Office Action mailed April 9, 2004. Reconsideration and allowance of the application and pending claims are respectfully requested.

I. Allowable Subject Matter

Applicant appreciates the Examiner's indication that claims 6 and 7 would be allowable if amended to overcome the rejections under 35 U.S.C. § 112, second paragraph, and rewritten to include all of the limitations of the base claim and any intervening claims.

In that it is believed that every rejection has been overcome, it is submitted that each of the claims that remains in the case is presently in condition for allowance.

II. Claim Rejections - 35 U.S.C. § 112

A. Rejections under 35 U.S.C. § 112, First Paragraph

Claims 1-12 have been rejected under 35 U.S.C. § 112, first paragraph, for the objections cited in the Office action against the specification. In particular, the Office Action alleges the following:

> Claims 1-12 are rejected under 35 U.S.C § 112, first paragraph, based on a disclosure which is not enabling. The "phase and frequency detector", the "charge pump", the "voltage controlled oscillator", the "current controlled oscillator" and the "loop filter" are deemed critical or essential to the practice of the invention for the circuit to be a "phase lock loop", but are not included in the claim(s). An arrangement lacking these features is not enabled by the disclosure since it cannot be understood from the specification how the circuit will operate without such. *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Applicants have amended the claims to recite a voltage-to-current converter. Additionally, Applicants have cancelled claims 9-15. In that the essential elements of the voltage-to-current converter are embodied in the amended claims, and in that claims 9-12 are among the claims cancelled, Applicants submit that the rejections to claims 1-12 under 35 U.S.C. § 112, first paragraph are rendered moot and respectfully request that the rejection of these claims under 35 U.S.C. § 112, first paragraph, be withdrawn.

B. Rejections under 35 U.S.C. § 112, Second Paragraph

Claims 1-15 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as their invention. In particular, the Office Action alleges the following (with no emphasis added by Applicants):

> Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
>
> In claim 1, it is not understood how the circuit can be a "phase lock loop" without the above discussed critical features. In lines 12-13, it is not understood what is meant by "voltages associated with the differential input signals" nor is there any element or means recited to provide this operation. It is not understood how the circuit can have this recited operation without any circuit to provide such.
>
> Claims 2-15 are rejected as including the indefiniteness discussed above with claim 1.
>
> In claim 9, it is not understood what is meant by "a voltage associated with the biasing signal". It is not understood what relevance this "voltage" has nor has it been recited as to where such is connected or provided in the circuit.
>
> Examiner has fully considered Applicant's remarks for the rejection to claim 9 and has not found them to be persuasive nor are such understood. It is not clear how the circuit can have a "voltage associated with the biasing signal" (emphasis added) without circuitry recited to provide such.

With regard to the arguments presented to claim 1 and claims 2-8, Applicants have amended the claims to recite a voltage-to-current converter in place of a phase lock loop, and thus respectfully submit that the rejection to claims 1-8 is rendered moot.

Additionally, in that claims 9-15 have been cancelled, Applicants respectfully submit that the rejection to claims 9-15 is rendered moot.

Also, Applicants have amended claim 8 and added claim 16 to further clarify one embodiment for providing the bias signal.

In view of the above described amendments to the claims, it is respectfully asserted that claims 1-8 and 16 currently define the invention in the manner required by 35 U.S.C. § 112. Accordingly, it is respectfully requested that the rejections to these claims be withdrawn.

III. Claim Rejections - 35 U.S.C. § 102(b)

A. Statement of the Rejection

Claims 1-5 and 8-21 have been rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by *Park, et al.* ("*Park*," U.S. Pat. No. 5,729,178). Applicants respectfully traverse this rejection, and understand the 35 U.S.C. § 102(b) rejection to encompass claims 1-5 and original claims 8-15 since claim 16 is newly added and because there are no claims beyond claim 16.

B. The *Park* Reference

Park discloses a fully differential folded cascode CMOS operational amplifier having adaptive biasing and common mode feedback, as indicated in the title. FIG. 8, which has been used in the Office Action, is a common mode feedback (CMFB) circuit. It has a parallel connection of pMOS and nMOS input stage amplifiers that extends the linear operation of the CMFB circuit, and thus enlarges the output voltage swing range of the operational amplifier shown in FIG. 5 of the reference. (See col. 8, line 40 and col. 9, lines 33-37.)

In contrast to Applicants' independent claim, *Park* does not disclose, teach, or suggest a "voltage-to-current converter **for use in a phase locked loop**" or a "voltage-to-current converter" that has "an input stage" including first and second switching transistors and first and second complementary transistors **arranged as part of a folded cascode configuration**, as presently recited in Applicants' independent claim 1. Additional distinctions will be described below.

C. Discussion of the Rejection

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of *each element* of the claim under consideration." *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983)(emphasis added). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102(b).

In the present case, not every feature of the claimed invention is represented in the *Park* reference. As an initial matter, *Park* does not disclose a "voltage-to-current

converter **for use in a phase locked loop**," as recited in the preamble. The Manual of Patent Examining Procedures, Section 2111.03 provides the following guidelines for evaluating preambles:

> Any terminology in the preamble that limits the structure of the claimed invention must be treated as a claim limitation....The claim preamble must be read in the context of the entire claim...During examination, statements in the preamble reciting the purpose or intended use of the claimed invention must be evaluated to determine whether the recited purpose or intended use results in a structural difference...between the claimed invention and the prior art. If so, the recitation serves to limit the claim.

Applicants submit that the phrase in the preamble, "for use in a phase locked loop" needs to be evaluated as a limitation to independent claim 1, as it results in a structural difference between independent claim 1 and *Park*. In other words, the structure illustrated in Figure 8 of *Park* is a common mode feedback circuit for providing a wide-common mode feedback for an operational amplifier, and not a voltage-to-current converter **for use in a phase locked loop**. Applicants respectfully submit that Park does not anticipate independent claim 1.

Additionally, *Park* does not disclose an "input stage," wherein "the first and the second switching transistors and the first and the second complementary transistors" are "arranged as part of a folded cascode configuration," as recited in independent claim 1. One skilled in the art would recognize the combination of the nMOS differential pair, pMOS transistors, and current mirror, interconnected as exemplified by one embodiment shown in FIG. 4, as a folded cascode configuration, which is a structural limitation not disclosed in the common mode feedback circuit of Figure 8 of *Park*. Thus, Applicants

submit that *Park* does not anticipate independent claim 1, and thus respectfully request that the rejection to claim 1 be withdrawn.

Because independent claim 1 is allowable over *Park*, dependent claims 2-8 and 16 are allowable as a matter of law for at least the reason that the dependent claims 2-8 and 16 contain all the elements of their respective base claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988)

In addition, Applicants also respectfully traverse the rejections of the dependent clams on other grounds. For example, *Park* does not disclose "a second output stage, wherein the output stage and the second output stage include a constant current source that provides a substantially constant current for the center frequency of the phase lock loop output when the difference between the differential input signals is substantially zero," as recited in dependent claim 4. The output in *Park* is a single-stage output, not a two-stage output. The Office Action alleges the following:

> Park et al. discloses, in Fig. 8, a circuit comprising: ... "an output stage" having "a first output stage (Mc5 and Mc12)" and "a second output stage Mc15 and Mc16)"; ... all connected and operating similarly as recited by Applicant.

Applicants respectfully disagree. Transistors Mc15 and Mc16 are configured in a differential-pair relationship with transistors Mc5 and Mc12, respectively. One skilled in the art would not recognize each half of a differential pair to be separate output stages, as alleged in the Office Action. Thus, *Park* does not disclose two output stages as recited in dependent claim 4, and therefore Applicants respectfully request that the rejection to dependent claim 4 be withdrawn.

As another example, Applicants submit that *Park* does not disclose "a biasing transistor coupled to a bias signal coupled to the output of a charge pump of the phase locked loop and to a supply voltage, wherein the biasing transistor is configured to generate a bias current for the first and second complementary transistors of the input stage," as recited in dependent claim 8. Neither a bias transistor nor a charge pump are disclosed in Figure 8 of *Park*, and thus Applicants respectfully request that the rejection to dependent claim 8 be withdrawn.

Due to these clear shortcomings of the *Park* reference, Applicants respectfully assert that *Park* does not anticipate Applicants' claims. Therefore, Applicants respectfully request that the rejection of these claims be withdrawn.

IV. Claim Rejections - 35 U.S.C. § 103(a)

Claims 13-15 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* (U.S. Pat. No. 5,889,437) in view of *Park*. As Applicants have cancelled claims 13-15 through amendment, Applicants respectfully submit that this rejection has been rendered moot.

V. Canceled Claims

As identified above, claims 9-15 have been canceled from the application through this response without prejudice, waiver, or disclaimer. Applicants reserve the right to present these canceled claims, or variants thereof, in continuing applications.

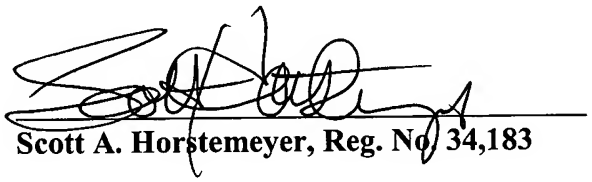
VI. New Claims

As identified above, claim 16 has been added into the application through this response. Applicants respectfully submit that this new claim further clarifies the circuitry that provides a bias signal described in claim 8.

CONCLUSION

Applicants respectfully submits that Applicants' pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Alexandria, Virginia 22313-1450, on

June 9, 2004.

Mary Megan

Signature